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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Pan et al.

Serial No.: 09/614,113

Filed: July 12, 2000

For: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH

Examiner: C. Brown

Group Art Unit: 1765

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APPLICANTS' APPEAL BRIEF

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BRIEF ON APPEAL

Hon. Assistant Commissioner of Patents
Washington, D.C. 20231
Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is in furtherance of the Notice of Appeal, filed in this case on June 19, 2002, and is submitted in triplicate in the format of 37 C.F.R. § 1.192(c), and with the fee required by 37 C.F.R. § 1.17(c).

(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc, assignee of the pending application as recorded with the United States Patent and Trademark Office on October 15, 1996, at Reel 8175, Frame 0501.

(2) RELATED APPEALS AND INTERFERENCES

Neither the appellants, the appellants' representative, nor the assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF THE CLAIMS

Claims 3 through 22 are pending in the application.

Claims 3 through 22 stand rejected.

Claims 3 through 22 are being appealed.

(4) STATUS OF AMENDMENTS

Applicants filed Remarks Under 37 C.F.R. § 1.116 on May 20, 2002, in response to the Final Office Action mailed February 22, 2002. Applicants did not seek to amend any claims by the Remarks in response to the Final Office Action. An Advisory Action mailed June 10, 2002, indicated that the request for reconsideration did not place the application in condition for allowance and that the rejection of the claims, as they currently stand in the application, is maintained.

(5) SUMMARY OF THE INVENTION

The present invention relates to a method for minimizing or eliminating damage to gate dielectric layers and/or silicon substrates during the formation of gate stack structures. *See,*

Specification at p. 4, lines 18-20. Damage to a gate dielectric layer and/or a silicon substrate may be caused by the formation of silicon clusters in metallic silicide films during fabrication of a gate stack structure. Specifically, it has been found that the pitting on a gate dielectric layer during gate stack etching processes is caused by the presence of silicon clusters inside metallic silicide films of the gate stack. *See, Specification* at p. 5, lines 25-27. High temperature gate stack fabrication steps (where temperatures exceed 600 °C) cause the formation of the damaging silicon clusters within an annealed or crystalline structured metallic silicide film. *Id.* at lines16-22. The present invention eliminates or hinders the formation of damaging silicon clusters in metallic silicide films by reducing the temperature during the fabrication of a gate stack structure. *See, Specification* at p. 4, lines 16-20. The elimination of the growth and formation of silicon clusters in a metallic silicide film eliminates the problem of pitting on the silicon substrate during a gate stack etch. *See, Specification* at p. 6, lines 3-5.

In the various embodiments of the present invention, a gate stack structure is formed by depositing a gate dielectric layer over a silicon substrate. A polysilicon layer is formed over the gate dielectric layer and implanted with impurities. A metallic silicide film is deposited on the polysilicon layer and a dielectric cap layer is deposited over the metallic silicide film. *See, Specification* at p. 8, lines 21-29. In accordance with the present invention, the fabrication of the dielectric cap layer of a gate stack structure is carried out between about 400 and 600 °C and preferably at about 500 °C. *See, Specification* at p. 6, lines 13-18; p. 8, line 29 – p. 9, line 4. The formation of the dielectric cap layer at the lower temperatures of between about 400 °C and 600 °C hinders or eliminates the formation of silicon clusters in the metallic silicide film. *See, Specification* at p. 6, lines 15-18. Thus, the formation of dielectric cap layers in accordance with the lower temperatures of the present invention prevents damage to the gate stack structure.

(6) ISSUES

Whether claims 3 through 22 are unpatentable under 35 U.S.C. § 103(a) over United States Patent 5,428,244, issued to Segawa et al., in view of United States Patent 5,438,006, issued to Chang.

(7) GROUPING OF CLAIMS

The grouping of the claims is as follows:

(a) Claim 3 stands and falls alone, reciting a method of forming a gate stack, including depositing a dielectric cap layer over a metallic silicide film at a temperature below about 600 °C which is not disclosed by the cited references.

(b) Claim 4 stands with claim 3 but falls alone because claim 4 recites the additional limitation of depositing a dielectric cap layer over the metallic silicide film at a temperature of between 400 °C and 600 °C which is not disclosed by the cited references.

(c) Claim 5 stands with claim 3 but falls alone because claim 5 recites the additional limitation of depositing a dielectric cap layer over the metallic silicide film at a temperature of about 500 °C which is not disclosed by the cited references.

(d) Claim 6 stands with claim 3 but falls alone because claim 6 recites the additional limitation of depositing a dielectric cap layer over the metallic silicide film at a temperature sufficiently low to maintain the metallic silicide film in a non-annealed state, which is not disclose by the cited references.

(e) Claim 7 stands with claim 3 but falls alone because claim 7 recites the additional limitation of depositing a dielectric cap layer over the metallic silicide film at a temperature

sufficiently low to preclude formation of silicon clusters in the metallic silicide film, which is not disclosed by the cited references.

(f) Claims 8 through 16 stand and fall with claim 3.

(g) Claim 17 stands and falls with claim 6.

(h) Claim 18 stands and falls with claim 3.

(i) Claim 19 stands and falls alone, reciting a method of forming a gate stack, including depositing a dielectric cap layer over the metallic silicide film at a temperature below about 600 °C such that the metallic silicide film remains in a non-annealed state, which is not disclosed by the cited references.

(j) Claim 20 stands and falls with claim 4.

(k) Claim 21 stands and falls with claim 5.

(l) Claim 22 stands and falls with claim 7.

(8) ARGUMENT

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. These criteria are detailed in Section 706.02(j) of the MPEP:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

The combination of Segawa et al. with Chang et al. fails to satisfy each of the requirements necessary to maintain a *prima facie* case of obviousness with respect to claim 3 through 22 of the

present invention. More specifically, the combination of Segawa et al. with Chang et al. fails to teach or suggest the formation of dielectric cap layers in a gate stack structure at the temperatures claimed by claims 3 through 22 of the present invention. The failure of the combined references to teach all of the claim limitations and satisfy the necessary requirements of a *prima facie* obviousness rejection precludes the present rejection under 35 U.S.C. § 103(a). Claims 3 through 22 should be allowed.

Segawa et al. discloses the formation of a gate stack structure, including a dielectric cap overlying a metallic silicide layer. In the *Official Action* mailed September 11, 2001 (*Official Action 1*) the Office admitted that Segawa et al. differed from the claimed invention. The claimed invention recited the limitation that the dielectric cap layer was deposited at a sufficiently low temperature which was not disclosed by Segawa et al. *See, Official Action 1* at p. 3, lines 3-4. The obviousness rejection, however, was maintained based upon the allegation that routine experimentation could have been used to optimize the effective variables, namely deposition temperatures.

In the *Official Action* mailed February 22, 2002 (*Official Action 2*) the obviousness rejection was restated, indicating that Segawa et al. included an example wherein "the two layers have the same deposition temperature." Reliance upon experimentation was eliminated from the stated reasons for the rejection. Instead, the rejection was based upon the unsupported assertion that "since both the silicon oxide layer and tungsten silicide layer are formed from the SH_2Cl_2 gas, the two layers have the same deposition temperature." *See, Official Action 2* at p. 3, lines 3-4. The disclosure of Segawa et al. does not support this allegation. Nowhere in the disclosure of Segawa et al. is there any indication that using SH_2Cl_2 gas to deposit both the tungsten silicide and silicon oxide layers produces equivalent deposition temperatures. In fact, Segawa et al.

specifically teaches that the deposition temperature used to form the dielectric cap layer is higher than the deposition temperature used to form the metallic silicide layer. The difference in the temperatures is confirmed by the statement that the two layers have "**almost** the same deposition temperature." *See, Segawa et al.* at col. 14, lines 7-8 (emphasis added). The inclusion of the term "almost" in the example of Segawa et al. directly opposes the allegation of the *Official Action 2* that the deposition temperatures disclosed by Segawa et al. are the same for the metallic silicide film and the dielectric cap layer. The fact that the deposition temperatures disclosed by Segawa et al. are not the same is admitted by the Office's statement that "the tungsten silicide film and the silicon oxide film almost have the same deposition temperature" as recited in the *Advisory Action* mailed June 10, 2002.

Furthermore, the disclosure of Segawa et al. specifically teaches that the deposition temperature of the tungsten silicide film and the silicon oxide layer are not the same. Even though a flow of SH_2Cl_2 gas to the CVD reaction chamber in Example VII of Segawa et al. is kept at a constant rate, the temperature within the reaction chamber is raised between the deposition of the tungsten silicide film and the deposition of the silicon oxide film. Specifically, "(1) the supply of WF_6 gas is brought to a halt, (2) at the same time, the chamber temperature is increased up to 650 °C to 700 °C, and (3) N_2O gas is introduced into the chamber at a flow rate of 0.4 to 0.6 lit. per minute (from t2 in FIG. 13)." *See, Segawa et al.* at col. 13, lines 55-59. The introduction of the N_2O gas, which initiates and is required for the deposition of the silicon oxide, does not occur until after the temperature within the deposition chamber is raised above 600 °C, specifically to a temperature between 650 °C and 700 °C. The fact that the temperature is above 600 °C for the deposition of the silicon oxide layer is further supported by FIG. 13 of Segawa et al. FIG. 13 clearly shows that prior to the time that the WF_6 flow ceases (time t1) the

temperature is being raised within the deposition chamber. At the time the flow of N_2O is initiated (time t2) the temperature is already well above 600 °C. Because N_2O must be present for the deposition of the silicon oxide, the earliest time at which the deposition of the Segawa et al. dielectric cap layer can begin is time t2. At time t2, the temperature in the deposition chamber is above 600 °C as disclosed by Example VII and illustrated in FIG. 13.

The disclosure of Chang et al. recites the formation of "a gate stack 32, comprising the patterned polysilicon layer 30 and the patterned metal layer 28, as opposed to a conventional gate stack, which also includes an overlying oxide layer." *See, Chang et al.* at col. 3, lines 4-8. A dielectric cap layer is not formed in the process of Chang et al. Furthermore, Chang et al. does not disclose any teaching or suggestion regarding the temperature at which a dielectric cap layer is disposed or formed over a metallic silicide film.

35 U.S.C. § 103(a) Rejection

(a) Claim 3

Claim 3 stands rejected over Segawa et al. in view of Chang et al. because the disclosure of deposition temperatures for a tungsten silicide film and a silicon oxide film which are "almost" the same allegedly reads on Applicants' claimed limitations of depositing a dielectric cap layer over the metallic silicide film at a temperature below about 600 °C. *See, Advisory Action.* Claim 3 stands and falls alone.

A *prima facie* obviousness rejection based upon the teachings of the combined references may only stand if the references "teach or suggest all of the claim limitations." *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)(emphasis added). Claim 3 specifically recites the limitation of "depositing a dielectric cap layer over said metallic silicide film at a temperature

below about 600 °C" (emphasis added). Such a limitation is neither taught nor suggested by the combined references. The failure of the combined references to teach or suggest this limitation precludes the outstanding obviousness rejection.

As detailed in the Remarks filed under 35 U.S.C. § 1.116, and *supra*, Segawa et al. fails to "teach or suggest" the deposition of a dielectric cap layer below about 600 °C as claimed by claim 3. Contrary to the assertion in the *Official Action 2*, Segawa et al. does not disclose the deposition of a silicon oxide (or dielectric cap layer) at the same temperature as that of the tungsten silicide layer. The comments in the *Advisory Action* acknowledge that Segawa et al. in fact discloses that the deposition temperature for the silicon oxide is "almost" the same as that of the tungsten silicide, but is not the same. The disclosure and Figures of Segawa et al. explicitly show that the deposition temperature used to deposit a silicon oxide layer is always above 600 °C. The deposition temperature for the dielectric cap layer of Segawa et al. never falls "below about 600 °C" as recited in claim 3. Even the graphs used to detail the deposition procedure of Segawa et al. clearly indicate that at time t2 (the time at which Segawa et al. teaches initiation of the N_2O gas flow for silicon oxide layer deposition), the deposition temperature is around 650 °C, well above the claimed "about 600 °C." *See, Segawa et al.* FIG. 13. Furthermore, the claimed temperature range is "below about 600 °C," not at or above about 600 °C. The deposition temperature of the silicon dioxide layer of Segawa et al. is initiated at about 650 °C but the deposition temperature continues to increase to about 700 °C. Thus, Segawa et al. actually teaches away from claim 3, indicating that the deposition temperature must be raised over 600 °C and should not be initiated until about 650 °C or 700 °C.

The combined references fail to teach or suggest the specific limitation recited in claim 3 of "depositing a dielectric cap layer over said metallic silicide film at a temperature below about

600 °C." The failure of the combined references to do so precludes the sustained obviousness rejection. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Claim 3 is allowable over the cited references.

(b) Claim 4

Claim 4 stands rejected over Segawa et al. in view of Chang et al. because the disclosure of deposition temperatures for a tungsten silicide film and a silicon oxide film which are "almost" the same allegedly reads on Applicants' claimed limitation of depositing a dielectric cap layer over the metallic silicide film at a temperature between 400 °C and 600 °C. Claim 4 stands with claim 3 but falls alone.

The combined references fail to disclose the limitation of depositing a dielectric cap layer over a metallic silicide film at a temperature of between 400 °C and 600 °C as claimed by claim 4. Segawa et al. specifically discloses a dielectric cap layer deposition temperature above 600 °C as previously discussed. Furthermore, Segawa et al. clearly states that the deposition temperature of the dielectric cap layer is raised to between 650 °C and 700 °C before N_2O gas is introduced into the deposition chamber to begin the deposition of the dielectric cap layer. *See, Segawa et al.* at col. 13, lines 54-59. Neither Segawa et al. nor Chang et al. ever indicate that a dielectric cap layer may be deposited at a temperature of between 400 °C and 600 °C as claimed by claim 4. The failure of the combined references to teach this claimed limitation precludes the establishment of a *prima facie* case of obviousness. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Claim 4 is allowable.

Furthermore, if claim 3 is allowed, claim 4 is also allowable as a dependent claim of an allowable independent claim. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir.

1988)(dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious).

(c) Claim 5

Claim 5 stands rejected over Segawa et al. in view of Chang et al. because the disclosure of deposition temperatures for a tungsten silicide film and a silicon oxide film which are "almost" the same allegedly reads on Applicants' claimed limitation of depositing a dielectric cap layer over the metallic silicide film at a temperature of about 500 °C. Claim 5 stands with claim 3 but falls alone.

In *Office Action 2* the Examiner pointed out that Segawa et al. discloses a deposition temperature for a tungsten silicide film of between 500 °C and 600 °C. The rejection of claim 5 is apparently maintained based upon the allegation that Segawa et al. teaches the same deposition temperature for both the metallic silicide film and the dielectric cap layer. However, Segawa et al. specifically indicate that the deposition temperature of the metallic silicide film and the dielectric cap layer are only "almost the same." *See, Segawa et al.* at col. 14, lines 5-8. This fact was acknowledged by the Examiner. *See, Advisory Action.* Thus, the original basis for rejecting claim 5 is admittedly flawed. Claim 5 should be allowed.

Furthermore, neither of the combined references discloses a deposition temperature for a dielectric cap layer at a temperature of about 500 °C as claimed by claim 5. At most, Segawa et al. discloses a deposition temperature for a dielectric cap layer of 650 °C or above. *See, Segawa et al.* at col. 13, lines 54-59; FIG. 13. The disclosure of a deposition temperature for a dielectric cap layer of 650 °C or more does not make obvious the claimed deposition temperature of about 500 °C. Claim 5 is therefore allowable over the 35 U.S.C. § 103(a) rejection. *See, In re Vaeck,*

947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In addition, if claim 3 is found to be allowable, claim 5 is also allowable as a dependent claim of a non-obvious independent claim. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)(dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious).

(d) Claim 6

Claim 6 stands rejected over Segawa et al. in view of Chang et al. because the disclosure of deposition temperatures for a tungsten silicide film and a silicon oxide film which are "almost" the same allegedly reads on Applicants' claimed limitation of depositing a dielectric cap layer over the metallic silicide film at a temperature sufficiently low to maintain said metallic silicide film in said non-annealed state. Claim 6 stands with claim 3 but falls alone.

The limitation claimed by claim 6 is not taught or suggested by the combined references. The Examiner acknowledged this fact in *Office Action 1* by stating that "Segawa differs from the claimed invention by specifying that the dielectric cap layer is deposited at a sufficiently low temperature." Because Segawa et al. admittedly fails to teach the limitation of a "temperature sufficiently low to maintain said metallic silicide film in said non-annealed state," Segawa et al. does not make obvious claim 6. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Office Action 1 also indicates that a person having ordinary skill in the art would have used the claimed limitation because routine experimentation is within the knowledge of one having such skill. Even if that is the case, claim 6 is not obvious because Segawa et al. teaches away from lowering the deposition temperature of a dielectric cap layer below about 650 °C.

Furthermore, Segawa et al. does not even acknowledge the fact that a dielectric cap layer may be deposited in a non-annealed state as claimed. Without a suggestion that it would be desirable to deposit a dielectric cap layer in a non-annealed state, there is no motivation for one having ordinary skill in the art to experiment and make obvious claim 6. Without any motivation, claim 6 is non-obvious. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The only motivation that does exist to form a dielectric cap layer in a non-annealed state is the Specification of the present invention. To use the Specification to motivate an obviousness rejection constitutes an improper use of hindsight. Claim 6 is allowable.

Furthermore, claim 6 is allowable over the 35 U.S.C. § 103(a) rejection if claim 3 is allowed because claim 6 depends from claim 3. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)(dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious).

(e) Claim 7

Claim 7 stands rejected over Segawa et al. in view of Chang et al. because the disclosure of deposition temperatures for a tungsten silicide film and a silicon oxide film which are "almost" the same allegedly reads on Applicants' claimed limitation of depositing a dielectric cap layer over the metallic silicide film at a temperature sufficiently low to preclude formation of silicon clusters in said metallic silicide film. Claim 7 stands with claim 3 but falls alone.

The combined references fail to teach or suggest the limitation of depositing a dielectric cap layer at a temperature sufficiently low to preclude formation of silicon clusters in a metallic silicide film. Neither Segawa et al. nor Chang et al. mention a way to preclude the formation of silicon clusters in a metallic silicide film. The failure to disclose such a limitation precludes a

prima facie obviousness rejection. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Similarly, there is no motivation to alter the lowest deposition temperature taught by Segawa et al. (650 °C) to deposit a dielectric cap layer at a temperature sufficiently low to preclude formation of silicon clusters in a metallic silicide film. The lack of motivation to alter the deposition temperature of the dielectric cap layer precludes a *prima facie* obviousness rejection. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Furthermore, if claim 3 is allowed, claim 7 is also allowable as a dependent claim of a non-obvious independent claim. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)(dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious).

(f) Claims 8 through 16

Claims 8 through 16 stand and fall with claim 3.

(g) Claim17

Claim 17 stands and falls with claim 6.

(h) Claim 18

Claim 18 stands and falls with claim 3.

(i) Claim 19

Claim 19 stands rejected over Segawa et al. in view of Chang et al. because the disclosure of deposition temperatures for a tungsten silicide film and a silicon oxide film which are

"almost" the same allegedly reads on Applicants' claimed limitation of "depositing a dielectric cap layer over said metallic silicide film at a temperature below about 600 °C such that the metallic silicide film remains in said non-annealed state." Claim 19 stands and falls alone.

As previously discussed, the combined references fail to disclose the formation of a dielectric cap layer at a temperature below about 600 °C as recited in claim 19. Segawa et al. only discloses the formation of a dielectric cap layer at a temperature of 650 °C or greater. Chang et al. does not discuss deposition temperatures for dielectric cap layers. The failure of the combined references to teach or suggest the deposition temperature limitation of below about 600 °C precludes a *prima facie* obviousness rejection under 35 U.S.C. § 103(a). *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Similarly, the combined references do not disclose the limitation of depositing a dielectric cap layer over a metallic silicide film at a temperature such that the metallic silicide film remains in a non-annealed state. Neither Segawa et al. nor Chang et al. even acknowledge that a dielectric cap layer may be formed such that the metallic silicide layer remains in a non-annealed state. The only teachings regarding a metallic silicide film layer having a non-annealed state originate with the Specification of the present invention. Thus, the claimed limitation is not taught by either of the references and there is no motivation to combine the references to make obvious the claimed limitation. Claim 19 is allowable over the standing rejection. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(j) Claim 20

Claim 20 stands and falls with claim 4.

(k) Claim 21

Claim 21 stands and falls with claim 5.

(l) Claim 22

Claim 22 stands and falls with claim 7.

CONCLUSION

Claims 3 through 22 are allowable over the 35 U.S.C. § 103 obviousness rejection and should be allowed for issue.

Respectfully submitted,

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APPENDIX

All claims currently pending and under consideration in this Appeal are shown below, in clean form, for clarity.

3. (Previously Amended) A method of forming a gate stack, comprising:

forming a gate dielectric layer on a silicon substrate;

forming a polysilicon layer on top of the gate dielectric layer;

subjecting said polysilicon layer to an ion implantation of impurities;

depositing a metallic silicide film in a non-annealed state atop said polysilicon layer; and

depositing a dielectric cap layer over said metallic silicide film at a temperature below about 600 °C.

4. The method of claim 3, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature of between 400 °C. and 600 °C .

5. The method of claim 3, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature of about 500° C.

6. The method of claim 3, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature sufficiently low to maintain said metallic silicide film in said non-annealed state.

7. The method of claim 3, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature sufficiently low to preclude formation of silicon clusters in said metallic silicide film.

8. The method of claim 3, further comprising forming said dielectric cap layer of silicon nitride.

9. The method of claim 3, further comprising forming said metallic silicide film as a cobalt silicide film.

10. The method of claim 3, further comprising forming said metallic silicide film as a molybdenum silicide film.

11. The method of claim 3, further comprising forming said metallic silicide film as a titanium silicide film.

12. The method of claim 3, further comprising forming said metallic silicide film as a tungsten silicide film.

13. The method of claim 3, further comprising forming said metallic silicide film as a silicon rich metallic silicide film.

14. The method of claim 3, further comprising forming said metallic silicide film with a non-crystalline structure.

15. The method of claim 3, wherein said depositing said dielectric cap layer over said metallic silicide film comprises selectively depositing silicon nitride by plasma-enhanced chemical vapor deposition.

16. The method of claim 3, wherein said depositing said dielectric cap layer is achieved using a deposition technique selected from the group consisting of chemical vapor deposition, sputtering, and spin-on techniques.

17. A method for forming a gate stack, comprising:

providing a semiconductor substrate with a dielectric layer on an active surface of said semiconductor substrate, wherein a polysilicon layer is disposed over said dielectric layer;

forming a metallic silicide film in a non-annealed state over said polysilicon layer;

forming a dielectric cap on said metallic silicide film at a sufficiently low temperature that said metallic silicide film remains in said non-annealed state;

forming and patterning a resist layer on said dielectric cap;

etching said dielectric cap, said metallic silicide film, and said polysilicon layer; and

stripping said resist layer.

18. The method of claim 17, wherein forming said dielectric cap is effected at a temperature below about 600° C.

19. A method of forming a gate stack, consisting essentially of:

forming a gate dielectric layer on a silicon substrate;

forming a polysilicon layer on top of the gate dielectric layer;

subjecting said polysilicon layer to an ion implantation of impurities;

depositing a metallic silicide film in a non-annealed state atop said polysilicon layer; and

depositing a dielectric cap layer over said metallic silicide film at a temperature below about 600 °C such that the metallic silicide film remains in said non-annealed state.

20. The method of claim 19, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature of between 400°C and 600°C.

21. The method of claim 19, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature of about 500°C.

22. The method of claim 19, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature sufficiently low to preclude formation of silicon clusters in said metallic silicide film.